Sierra Components, Inc.

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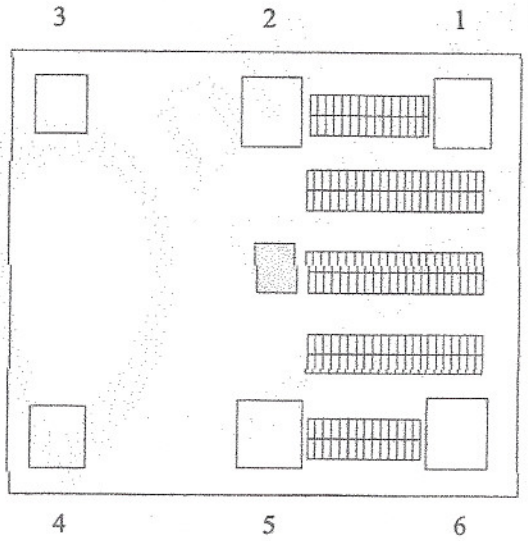
PAD FUNCTIONS

1	V_{IN}
2	V_{OUT}
3	V_{OUT}
4	ADJ
5	V_{OUT}
6	V_{IN}



NOTE: SHADED PAD IS NOT TO BE BONDED

The information given is believed to be correct at the time of issue.
Please verify your requirements prior to commencement of any assembly process, as no liability for omission or error can be accepted.
Chip back potential is the level at which bulk silicon is maintained either by bond pad connection or in some cases the potential to which the chip back must be connected if stated above.

Note: 1 mil = 0.001inch

APPROVED GB ..... DATE: 27/05/2008	LM117 FAIRCHILD SEMICONDUCTOR	DIE INFORMATION DIMENSIONS (Mils): 94 x 82 x 16 BOND PADS (Mils): 7.9 x 11 (Min.) MASK REF: GEOMETRY: BACK POTENTIAL:
DG 10.1.2 **Rev B, 7/19/02**		METALLISATION TOP: Al BACK: Va/Ni/Ag